In re Patent Application of:
DEQUINA ET AL
Serial No. **10/725,764**
Filed: **12/2/03**

In the Claims:

Please amend the claims as follows:

1. - 11. (Currently Canceled)

12. (New) A control circuit for a switch mode DC-DC converter comprising an arrangement of LGATE, UGATE and PHASE node condition threshold detectors, said LGATE condition threshold detector being operative to monitor the gate (LGATE) of a lower FET (LFET), said UGATE condition threshold detector being operative to monitor the gate (UGATE) of an upper FET (UFET), and said PHASE node condition threshold detector being operative to monitor the PHASE or common node between said UFET and said LFET, outputs of said threshold detectors being processed in accordance with a switching control operator to ensure that each of said UFET and said LFET is completely turned off before the other FET begins conduction, thereby maintaining a dead time that exhibits no shoot-through current and is independent of the type of switching FET, and wherein, said switching control operator is operative to trigger turn-on of said UFET, which causes the phase node voltage to go high, subsequent to turn off of said LFET, and in response to the voltage at said PHASE node having reached a prescribed negative polarity voltage following a predetermined blanking delay.

13. (New) The control circuit according to claim 12, wherein, in the absence of said PHASE node having reached said prescribed negative polarity voltage subsequent to the LGATE voltage going low, and in response to said PHASE node having reached prescribed positive threshold following a blanking delay, said switching control operator is operative to trigger turn-on of the UFET, which causes the phase node voltage to go high.

14. (New) The control circuit according to claim 13, wherein, in response to the elapse of a prescribed time-out without either of prescribed positive and negative polarity thresholds having been reached at said phase node following a blanking delay, said switching control operator is operative to trigger turn-on of the UFET, so that the voltage at the phase node goes high.

15. (New) The control circuit according to claim 12, wherein, subsequent to turn-off of said UFET, and in response to the UGATE voltage dropping to a voltage level that is a prescribed value above the phase voltage, said switching control operator is operative to trigger a prescribed time out before turning on said LFET.

16. (New) The control circuit according to claim 15, wherein, subsequent to turn-off of said UFET, and in response to the level of the PHASE node voltage reaching a predetermined

threshold voltage, said switching control operator is operative to turn on said LFET.

17. (New) A method for controlling a switch mode DC-DC converter comprising an upper FET (UFET), the gate of which is an upper gate (UGATE), and a lower FET (LFET) the gate of which is a lower gate (LGATE), said UFET and said LFET being coupled between power supply voltage rails, and having a common or PHASE node therebetween, said method comprising the steps of:

(a) monitoring LGATE, UGATE and PHASE node voltages; and

(b) subsequent to turn off of said LFET, and in response to the voltage at the PHASE node having reached a prescribed negative polarity voltage following a predetermined blanking delay, triggering turn-on of the UFET, so as to cause said phase node voltage to go high.

18. (New) The method according to claim 17, wherein step (b) further comprises, in the absence of said PHASE node having reached said prescribed negative polarity voltage subsequent to the LGATE voltage going low, and in response to said PHASE node having reached prescribed positive threshold following a blanking delay, triggering turn-on of said UFET, so as to cause said phase node voltage to go high.

19. (New) The method circuit according to claim 18, wherein step (b) further comprises, in response to the elapse of a prescribed time-out without either of prescribed positive and

negative polarity thresholds having been reached at said phase node following a blanking delay, triggering turn-on of said UFET, so that the voltage at said phase node goes high.